# FDS6680A

## Single N-Channel, Logic Level, PowerTrench® MOSFET

### General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor’s advanced Power Trench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

### Features

- 12.5 A, 30 V $R_{DS(ON)} = 9.5 \, \text{m} \Omega$ @ $V_{GS} = 10$ V
- $R_{DS(ON)} = 13 \, \text{m} \Omega$ @ $V_{GS} = 4.5$ V
- Ultra-low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

### Pinout

[Diagram](image)

### Absolute Maximum Ratings

$T_a=25^\circ\text{C}$ unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
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<tbody>
<tr>
<td>$V_{DSS}$</td>
<td>Drain-Source Voltage</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GSS}$</td>
<td>Gate-Source Voltage</td>
<td>±20</td>
<td>V</td>
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<tr>
<td>$I_D$</td>
<td>Drain Current – Continuous</td>
<td>12.5</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>– Pulsed</td>
<td>50</td>
<td></td>
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<tr>
<td>$P_D$</td>
<td>Power Dissipation for Single Operation</td>
<td>(Note 1a)</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td>(Note 1b)</td>
<td>(Note 1b)</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>(Note 1c)</td>
<td>(Note 1c)</td>
<td>1.0</td>
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<tr>
<td>$T_J, T_{STG}$</td>
<td>Operating and Storage Junction Temperature Range</td>
<td>–55 to +150</td>
<td>°C</td>
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</tbody>
</table>

### Thermal Characteristics

- $R_{JA}$ Thermal Resistance, Junction-to-Case (Note 1a) 50 °C/W
- $R_{JC}$ Thermal Resistance, Junction-to-Case (Note 1) 25 °C/W

### Package Marking and Ordering Information

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<th>Device</th>
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<th>Tape width</th>
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<td>FDS6680A</td>
<td>13''</td>
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### Electrical Characteristics 

_T_a = 25°C unless otherwise noted_

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<th>Symbol</th>
<th>Parameter Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
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<td><strong>Off Characteristics</strong></td>
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<td><em>BV_DSS</em></td>
<td>Drain–Source Breakdown Voltage</td>
<td>V_GS = 0 V, I_D = 250 µA</td>
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<td></td>
<td>V</td>
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<td><em>ΔBV_DSS</em></td>
<td>Breakdown Voltage Temperature Coefficient</td>
<td>I_D = 250 µA, Referenced to 25°C</td>
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<td>mV/°C</td>
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<td><em>I_DSS</em></td>
<td>Zero Gate Voltage Drain Current</td>
<td>V_GS = 24 V, V_DS = 0 V</td>
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<td></td>
<td></td>
<td>µA</td>
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<td><em>I_GSS</em></td>
<td>Gate–Body Leakage</td>
<td>V_GS = ±20 V, V_DS = 0 V</td>
<td>±100</td>
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<td></td>
<td>nA</td>
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<td><strong>On Characteristics</strong></td>
<td>(Note 2)</td>
<td></td>
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<td></td>
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<tr>
<td><em>V_GS(th)</em></td>
<td>Gate Threshold Voltage</td>
<td>V_DS = V_GS, I_D = 250 µA</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>V</td>
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<tr>
<td><em>ΔV_GS(th)</em></td>
<td>Gate Threshold Voltage Temperature Coefficient</td>
<td>I_D = 250 µA, Referenced to 25°C</td>
<td>−4.9</td>
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<td>mV/°C</td>
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<td><em>R_DS(on)</em></td>
<td>Static Drain–Source On–Resistance</td>
<td>V_GS = 10 V, I_D = 12.5 A</td>
<td>7.8</td>
<td>9.5</td>
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<td>mΩ</td>
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<td><em>I_D(on)</em></td>
<td>On–State Drain Current</td>
<td>V_GS = 10 V, V_DS = 5 V</td>
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<td><em>g_FS</em></td>
<td>Forward Transconductance</td>
<td>V_GS = 15 V, I_D = 12.5 A</td>
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<td><strong>Dynamic Characteristics</strong></td>
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<tr>
<td><em>Ciss</em></td>
<td>Input Capacitance</td>
<td>V_GS = 15 V, V_DS = 0 V</td>
<td>1620</td>
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<td><em>Coss</em></td>
<td>Output Capacitance</td>
<td>f = 1.0 MHz</td>
<td>380</td>
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<td><em>Crss</em></td>
<td>Reverse Transfer Capacitance</td>
<td>V_GS = 0 V, V_DS = 0 V, f = 1.0 MHz</td>
<td>160</td>
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<td>pF</td>
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<td><em>R_G</em></td>
<td>Gate Resistance</td>
<td>V_GS = 15 V, f = 1.0 MHz</td>
<td>1.3</td>
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<td>Ω</td>
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<td><strong>Switching Characteristics</strong></td>
<td>(Note 2)</td>
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<td><em>t_d(on)</em></td>
<td>Turn–On Delay Time</td>
<td>V_G = 15 V, I_D = 1 A, R_GEN = 6 Ω</td>
<td>10</td>
<td>19</td>
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<td><em>t_r</em></td>
<td>Turn–On Rise Time</td>
<td>V_GS = 10 V,</td>
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<td>10</td>
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<td><em>t_d(off)</em></td>
<td>Turn–Off Delay Time</td>
<td>V_GS = 5 V,</td>
<td>27</td>
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<td><em>t_f</em></td>
<td>Turn–Off Fall Time</td>
<td>V_GS = 15 V,</td>
<td>15</td>
<td>27</td>
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<td><em>Q_g</em></td>
<td>Total Gate Charge</td>
<td>V_GS = 15 V, I_D = 12.5 A,</td>
<td>16</td>
<td>23</td>
<td></td>
<td>nC</td>
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<tr>
<td><em>Qgs</em></td>
<td>Gate–Source Charge</td>
<td>V_GS = 5 V</td>
<td>5</td>
<td></td>
<td></td>
<td>nC</td>
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<td><em>Qgd</em></td>
<td>Gate–Drain Charge</td>
<td>V_GS = 0 V,</td>
<td>5.8</td>
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<td></td>
<td>nC</td>
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<td><strong>Drain–Source Diode Characteristics and Maximum Ratings</strong></td>
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<td><em>I_S</em></td>
<td>Maximum Continuous Drain–Source Diode Forward Current</td>
<td>2.1</td>
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<td>A</td>
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<td><em>V_SD</em></td>
<td>Drain–Source Diode Forward Voltage</td>
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<td>0.73</td>
<td>1.2</td>
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<td>V</td>
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<tr>
<td><em>T_r</em></td>
<td>Diode Reverse Recovery Time</td>
<td>I_R = 12.5 A, dV/dt = 100 A/µs</td>
<td>28</td>
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<td>ns</td>
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<td><em>Q_rr</em></td>
<td>Diode Reverse Recovery Charge</td>
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<td>nC</td>
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**Notes:**

1. _R_{θJA}_ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. _R_{θJC} is guaranteed by design while _R_{θCA} is determined by the user's board design.

   a) 50°C/W when mounted on a 1in² pad of 2 oz copper
   b) 105°C/W when mounted on a .06 in² pad of 2 oz copper
   c) 125°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%
Typical Characteristics

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.
Typical Characteristics

- **Figure 7. Gate Charge Characteristics.**
  - $i_D = 12.5A$
  - $V_{DS} = 10V$
  - $V_{GS} = 20V$

- **Figure 8. Capacitance Characteristics.**
  - $C_{oss} = 1MHz$

- **Figure 9. Maximum Safe Operating Area.**
  - $V_{GS} = 0V$
  - $R_{DS(ON)} = 125°C/W$
  - $T_J = 25°C$

- **Figure 10. Single Pulse Maximum Power Dissipation.**
  - $P_{(pk)} = R_{DS(ON)}$ * $T_J$
  - Duty Cycle, $D = t_1 / t_2$

- **Figure 11. Transient Thermal Response Curve.**
  - Thermal characterization performed using the conditions described in Note 1c.
  - Transient thermal response will change depending on the circuit board design.
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<th>Definition</th>
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